PATENT APPLICATION
Attorney's Doc. No. 9898-204
Client No. SS-16038-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jae-Yoon SIM and Jei-Hwan YOO

Serial No.: 09/901,930 Group Art Unit: 2816

Filed: July 9, 2001 Examiner: Cunningham, Terry D.

For: NEGATIVE VOLTAGE GENERATOR FOR A SEMICONDUCTOR MEMORY DEVICE

Confirmation No. 7100

ATTENTION: Board of Patent Appeals and Interferences
Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

This Appeal Brief is in furtherance of the Notice of Appeal mailed in this case on April 21, 2003. Appeal is taken from the Office Action mailed February 20, 2003 that finally rejected claims 1-24.

The fees required under §1.17(c) and any required petition for extension of time for filing this Brief and fees therefore are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This Brief is transmitted in triplicate.

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REAL PARTY IN INTEREST

The present application has been assigned to the following party:

Samsung Electronics Co., Ltd.
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Republic of Korea

RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the Applicant, or to the Applicant's legal representative.

STATUS OF CLAIMS

Claims in the application: 1-63

Claims withdrawn from consideration but not cancelled (non-elected): 25-63

Claims canceled: None

Claims allowed: None

Claims pending: 1-24

Claims rejected: 1-24 (of all of which are finally rejected)

Claims appealed: 1-24

STATUS OF AMENDMENTS

The claims have not been amended and remain as originally filed on July 9, 2001.

SUMMARY OF THE INVENTION

Embodiments of the invention provide an apparatus and method for an improved negatively biased word line scheme. Advantages found in embodiments of the invention include a reduced response time, reduced output ripple, and reduced sensitivity to process and temperature variations. (page 20, lines 3-12).

ISSUES

Whether claims 1, 7, 12, and 13 are anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 4,961,007 to Kumanoya et al. ("Kumanoya").

Whether claims 1-24 are unpatentable under 35 U.S.C. 103(a) based on U.S. Patent No. 6,052,022 to Lee ("Lee") in view of U.S. Patent No. 5,600,551 to Luscher, Jr. ("Luscher").

GROUPING OF CLAIMS

35 U.S.C. § 102(b) rejections (claims 1, 7, 12, and 13): Independent claims 1 and 7

stand and fall together. Claims 12 and 13 depend from claim 7.

35 U.S.C § 103(a) rejections (claims 1-24): Independent claims 1, 7, and 17 stand and fall together. The Applicants believe that independent claim 14 is allowable for additional reasons beyond those presented for claims 1, 7, and 17.

ARGUMENT

The refresh time of a memory cell is degraded by the leakage current of the access transistor (specification, page 1, lines 14-15). Conventional negatively biased word line schemes are intended to reduce the leakage current by applying a negative voltage to the word lines of non-selected memory cells (specification, page 1, lines 15-18). A negative word line scheme requires large current drive capability to discharge a word line from a boosted voltage to a negative voltage during a word line precharge operation (specification, page 2, lines 7-10). The present invention provides an apparatus and method for an improved negative word line biasing scheme.

Claims 1, 7, 12, and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kumanoya. Claims 1 and 7 recite a second charge pump and a second charge pumping means, respectively, that are adapted to be controlled by a precharge signal. Claims 12 and 13 inherently contain the limitations of claim 7.

Of key importance is whether the "RAS signal" disclosed by Kumanoya (FIG. 4) is equivalent to the "precharge signal" of claims 1 and 7. The Applicants have previously argued that Kumanoya's RAS signal is used to initiate an access operation for a ***selected memory cell*** (col. 4, lines 1-5, emphasis added). In contrast, the Applicant's precharge signal is used to return a word line to a negative voltage state after an access operation is completed, thereby reducing leakage current in ***non-selected memory cells*** (specification, page 1, lines 14-18, emphasis added). In the final rejection, the Examiner found this reasoning to be non-persuasive as reading upon operations or elements not recited in the claims, subsequently giving the claims what the Examiner considered to be their broadest reasonable interpretation (page 2, final paragraph). The Examiner explained in the final rejection that because Kumanoya's RAS signal provides an "initial state" to the oscillator, it is reasonable to consider the RAS signal a precharge signal.

A telephonic interview was held with the Examiner on May 12, 2003, to clarify what was meant by "providing an initial state." At this time the Examiner reiterated that because Kumanoya's RAS signal provides an "initial state" to the oscillator, the RAS signal is

reasonably considered a "precharge signal" within the context of pending claims 1 and 7.

The Applicants disagree, and believe that the Examiner has overly generalized the claimed precharge signal in a way that is inconsistent with the specification. Any "signal" may be said to provide an initial state to a device that uses the signal as input. The fact that Applicant claims a "precharge signal" is sufficient to distinguish over Kumanoya's "RAS signal" for the following reasons.

Pending claims must be given the broadest reasonable interpretation consistent with the specification (MPEP 2111). The specification defines a precharge signal as any suitable command and/or signal ***that corresponds to a precharge operation for a word line or any other type of memory access line that operates with a negative precharge voltage*** (specification, page 5, lines 28-32, emphasis added). A precharge operation is the discharge of a word line from a boosted voltage to a negative voltage (specification, page 2, lines 7-10). This occurs when a negative voltage is applied to the word lines of ***non-selected memory cells*** (specification, page 1, lines 16-18, emphasis added). FIG. 3 of the specification illustrates the periodic discharge of a word line from a boosted voltage to a negative voltage (see "charge pumping" segment) to counteract the leakage current. The leakage current degrades the refresh time of a memory cell (specification, page 1, lines 14-15).

On the other hand, Kumanoya's RAS signal indicates the operation state of the semiconductor memory device (column 6, lines 19-22). When RAS is high (the semiconductor memory device is selected and in an operational state), Kumanoya's second charge pump becomes operational and a bias potential is applied to the substrate (column 8, lines 29-55). Because Kumanoya's RAS signal does not correspond to a precharge operation for a memory access line of non-selected memory cells, it is not analogous to the Applicants' precharge signal.

For at least these reasons, the Applicants submit that claims 1, 7, 12, and 13 are not anticipated by Kumanoya.

Claims 1-24 also stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Luscher. As previously indicated, claims 1 and 7 recite a second charge pump and a second charge pumping means, respectively, that are adapted to be controlled by a precharge signal. Claim 14 recites a second charge pump that is adapted to be controlled by a word-line precharge signal. Claim 17 recites controlling a negative voltage generator responsive to a precharge signal. In light of the definition for "precharge signal" found in the specification that was discussed above, the terms "word-line precharge signal" (claim 14) and

"precharge signal" (claims 1, 7, 17) are substantially interchangeable.

Similar to the discussion above regarding Kumanoya, the Applicants do not believe that Lee discloses the element of a precharge signal, an element which the Examiner alleges is disclosed by the signal "RASB" shown in FIGURE 1.

A closer inspection reveals that Lee's RASB signal is more akin to Kumanoya's RAS signal. Lee's complementary row-address strobe (RASB) is a clock signal that indicates a standby mode when high and an active mode when low (column 1, lines 50-54). Lee's active kicker circuit 12A (FIG. 1) is enabled in the active state when RASB is at a low level (column 1, lines 56-59). Because Lee's RASB signal does not correspond to a precharge operation for a memory access line of non-selected memory cells, it does not teach or disclose the Applicant's precharge signal. Even if Luscher can be said to teach the limitation that the Examiner describes in the final rejection, the combination of Lee and Luscher still lack the recited limitation of control by a precharge signal. Consequently, the Lee/Luscher combination does not establish a *prima facie* case of obviousness for this reason.

Further in regard to claim 14, it recites a first charge pump that produces a first negative voltage as an output. Claim 14 also recites a negative voltage regulator with an input coupled to the output of the negative voltage generator and an output for generating a second negative voltage responsive to the first negative voltage. The Applicants note at this time that it appears that the "negative voltage generator" found in the claim 1 phrase "a negative voltage regulator with an input coupled to the output of the negative voltage generator" is a mistake and should be replaced with "the first charge pump."

This mistake does not affect the substance of the Examiner's final rejection in any way, where it is alleged that the claimed negative voltage regulator is shown by clamping section 15 in Lee's FIG. 1, and where it is also alleged that the input and output of clamping section 15 is the same terminal.

The Applicants disagree with the Examiner for the following reasons. According to Lee, the clamping section 15 prevents the high on-chip voltage Vpp from rising over a predetermined level by "sinking" excessive charges generated during pumping to the supply voltage line if the high voltage Vpp becomes greater than the predetermined level (column 2, lines 11-15). Consequently, Lee's high on-chip voltage Vpp is not a first negative voltage as recited in claim 14. Additionally, by reciting both "an input" and "an output" for the claimed voltage regulator, one of ordinary skill would assume that the voltage regulator has an input and an output that are separate and distinct. If the clamping section 15 indeed has a single

terminal that is both the input and the output, then it does not meet the recited claim 14 limitation of "generating a second negative voltage responsive to the first negative voltage." Since the voltage Vpp is generated by the first charge pumping circuit 11B (FIG. 1), the clamping section does not generate Vpp but merely prevents it from exceeding a certain level. Similarly, claim 14 recites a "first negative voltage" and a "second negative voltage," with the implication that the first and second negative voltages are separate and distinct. Conversely, if Vpp shown in Lee FIG. 1 is both the input and the output for the clamping section 15, then Lee fails to teach or disclose both a first and a second negative voltage because Vpp remains Vpp at all times.

Consequently, the Lee/Luscher combination fails to establish a *prima facie* case of obviousness with respect to claim 14 for this reason as well.

CONCLUSION

The Applicants respectfully request that the rejections of claims 1-24 be reversed and the application be returned to the Examiner to carry into effect the Board's decision.

Respectfully submitted,
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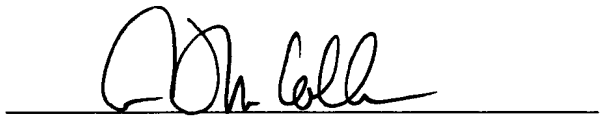

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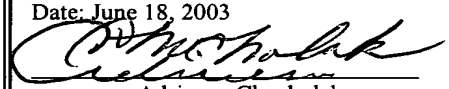

Adrienne Chocholak

APPENDIX

Claims 1-24 of the present application read as follows:

1. A negative voltage generator for a semiconductor memory device comprising:

a first charge pump having an output; and

a second charge pump having an output coupled to the output of the first charge pump, wherein the second charge pump is adapted to be controlled by a precharge signal.

2. A negative voltage generator according to claim 1 further comprising a negative voltage regulator having an input coupled to the output of the first charge pump and an output coupled to the output of the second charge pump.

3. A negative voltage generator according to claim 1 wherein the output of the first charge pump is connected directly to the output of the second charge pump.

4. A negative voltage generator according to claim 3 further comprising a negative voltage regulator having an input coupled to the outputs of the first and second charge pumps.

5. A negative voltage generator according to claim 1 further comprising a level detector having an input coupled to the output of the first negative charge pump.

6. A negative voltage generator according to claim 1 wherein the precharge signal is a word-line precharge signal.

7. A negative voltage generator for a semiconductor memory device comprising:

first means for pumping charge to a negative voltage source; and

second means for pumping charge to the negative voltage source, wherein the second means for pumping charge is adapted to be controlled by a precharge signal.

8. A negative voltage generator according to claim 7 wherein the first means for pumping charge has an output connected directly to an output of the second means for

pumping charge.

9. A negative voltage generator according to claim 7 further comprising means for regulating the negative voltage source.

10. A negative voltage generator according to claim 9 wherein:

the first means for pumping charge has an output connected directly to an output of the second means for pumping charge; and

the means for regulating the negative voltage source has in input coupled to an output of the first means for pumping charge and an output of the second means for pumping charge.

11. A negative voltage generator according to claim 9 wherein the means for regulating the negative voltage source has in input coupled to an output of the first means for pumping charge and an output coupled to an output of the second means for pumping charge.

12. A negative voltage generator according to claim 7 further comprising means for detecting the voltage level of the negative voltage source.

13. A negative voltage generator according to claim 7 wherein the negative voltage source is a negative voltage source for negatively biasing a word line.

14. A negative voltage generator for a semiconductor memory device comprising:

an oscillator;

a first charge pump having an input coupled to the oscillator and an output for generating a first negative voltage responsive to an oscillating signal from the oscillator;

a negative voltage regulator having an input coupled to the output of the negative voltage generator and an output for generating a second negative voltage responsive to the first negative voltage; and

a second charge pump having an output coupled to the output of the negative voltage regulator, wherein the second charge pump is adapted to be controlled by a word-line precharge signal.

15. A negative voltage generator according to claim 14 further comprising a level

detector having an input coupled to the output of the first charge pump and an output coupled to the oscillator.

16. A negative voltage generator according to claim 14 wherein the second charge pump is adapted to pump a predetermined amount of charge to the second negative voltage responsive to the word-line precharge signal.

17. A method for operating a semiconductor memory device comprising controlling a negative voltage generator responsive to a precharge signal.

18. A method according to claim 17 wherein:

the negative voltage generator comprises a first charge pump and a second charge pump; and

controlling a negative voltage generator responsive to a precharge signal comprises activating the second charge pump responsive to the precharge signal.

19. A method according to claim 18 wherein the first charge pump generates a first negative voltage.

20. A method according to claim 19 wherein activating the second charge pump responsive to the precharge signal comprises coupling charge from the second charge pump to the first negative voltage.

21. A method according to claim 19 further comprising regulating the first negative voltage, thereby generating a second negative voltage.

22. A method according to claim 21 wherein activating the second charge pump responsive to the precharge signal comprises coupling charge from the second charge pump to the second negative voltage.

23. A method according to claim 18 wherein activating the second charge pump responsive to the precharge signal comprises supplying a predetermined amount of charge from the second charge pump.

24. A method according to claim 17 wherein the precharge signal is a word-line precharge signal.